CASTOR design:
- Forward (5.2 < η < 6.6) Čerenkov quartz-tungsten sampling calorimeter - compact, radiation hard and fast
- CASTOR consists of 16 azimuthal sectors (semi-octants) mechanically organized in two half calorimeters;
- Each sector is divided longitudinally in electromagnetic (EM) and hadronic (HAD) modules: 2xEM+12xHAD
  - 2 x EM = 0.77 λ = 20 X₀
  - 12 x HAD = 12 x 0.77 λ
  - total depth = 13 x 0.77 λ = 10λ
- 5 sampling units (quartz+W) per each module

CASTOR installation in CMS:
- CASTOR installed on collar table of HF platform (-Z side) in June 2009
- CMS magnet tests at 3.8 T successful
- commissioned with LED (>90% of good channels)

CMS DAQ and CASTOR integration
- based on CERN developed xDAQ framework (C++)
- control via Run Control and Monitor System for CMS Experiment based on Tomcat/Ajax

CASTOR installation in CMS
- CASTOR installation in CMS
- CMS DAQ monitor
- on basis of HCAL DAQ
- fully integrated in CMS DAQ

Signal Digitization:
- based on HCAL Forward (HF) Readout BoX (RBX)
- signal from PMT is digitized with a QIE chip
  - fast (40 MHz) nonlinear FlashADCs
  - 32 bins (5 bit) with different weights and 4 ranges
  - dynamic range of 10,000 from 2.6 fC/bin 26 pC/bin
- one QIE module for 6 read-out channels

Per a QIE module:
- 3 CCA chips (Channel Control ASIC)
  - data compression and synchronisation
  - clock to QIE chips
- 2 GOL (Gigabit Optical Link)
  - data flow: transformation from parallel to serial
- VCSEL (Vertical Cavity Surface Emitting Laser) 1.6 Gb/s laser (32 bit @ 40 MHz)
  - 3 CCA chips (Channel Control ASIC)
  - control of QIE chips

Data to Surface
3 data streams to the CMS Front-End Drivers (FED), one DCC to one FED

Read-Out:
- 13 (12) QIE modules controlled with a one Clock Control and Monitoring Module (CCM) - three crates providing 228 channels
  - one calibration unit with 8 LEDs for PMT calibration/monitoring (1 common LED per two sectors)
- 6 Hcal Trigger Readout (HTR) boards
  - 16 input channels = 48 readout channels per each HTR
  - data re-forming, storing data during L1 latency, integrity check, trigger decision
- 3 Data Concentrator Cards (DCC)
  - 3 data streams to the CMS Front-End Drivers (FED), one DCC to one FED

CASTOR trigger bits
- HTR (3 input channels/12 readout channels) CASTOR trigger bit
- Data Concentrator Card (DCC)
- Producing triggering input