Upgrade of the PreProcessor System for the ATLAS LVL1 Calorimeter Trigger: from ASICs to FPGA

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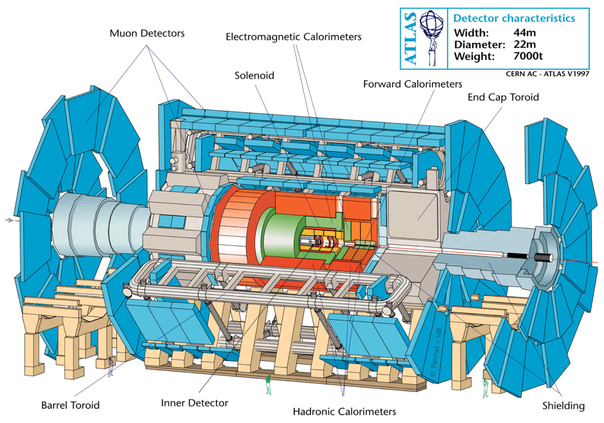
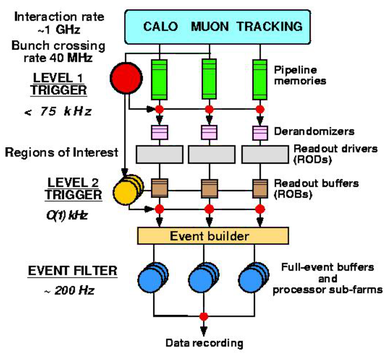
PHYSICS AT THE TERA SCALE
Helmholtz Alliance

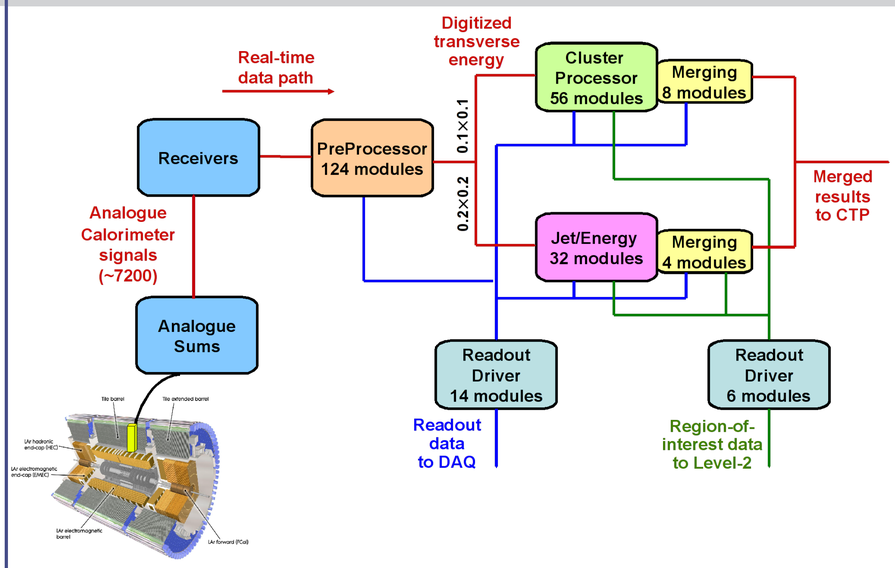
The ATLAS Experiment





ATLAS is a multipurpose experiment designed for the LHC.
3-Level trigger system is used to reduce data rates from $40MHz$ to $\sim 200Hz$.
Custom designed processors (ASIC and FPGA based) used at LVL1 to make a fast ($< 2\mu s$) decision with limited resolution.

ATLAS Level-1 Calorimeter Trigger

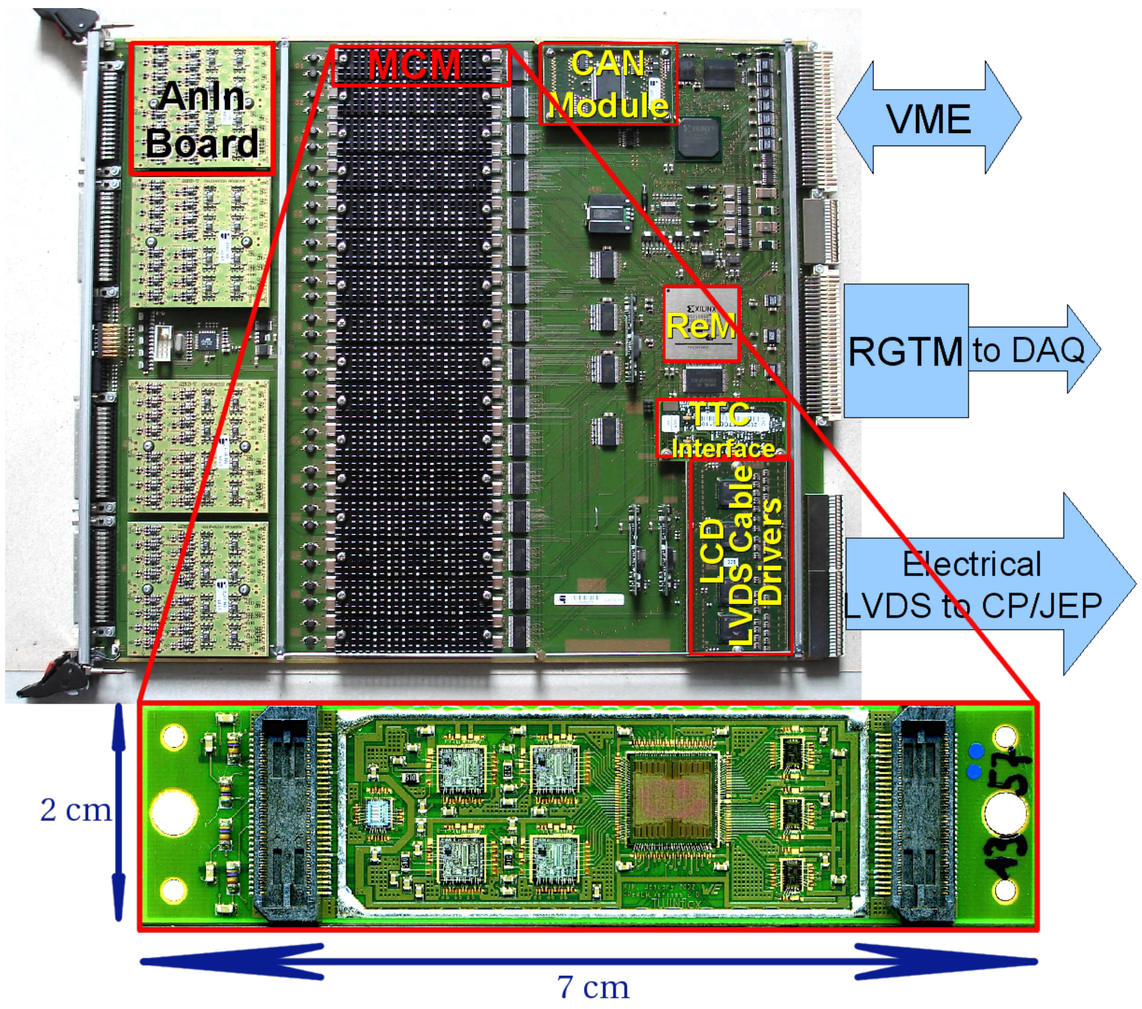


Based on Trigger Towers i.e. presummed Calorimeter signals
Two step system:

- **Preprocessing**: Digitisation and Bunch Crossing Identification
- **Processing**: Search for electron, jet and tau candidates, determination of $MissingE_T$ and $SumE_T$

Features of the Real-time Data Path:
Fixed Latency ($\sim 1\mu s$); Pipeline processing; Massive parallelism;

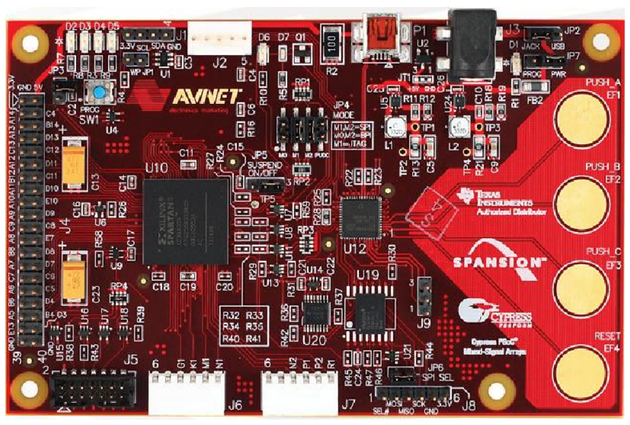
The PreProcessor System: 124 PreProcessor Modules

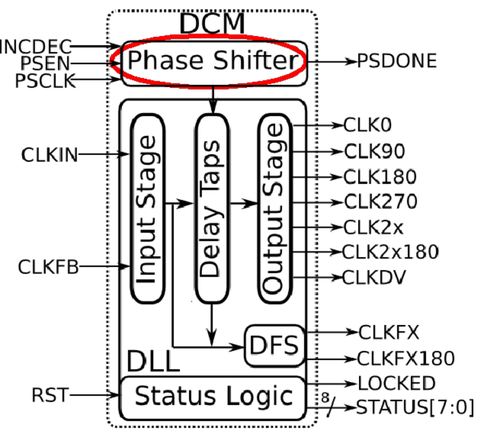


Processing is performed on a Multi Chip Module (MCM):

- 10(12)-bit, 40 MHz, 3 BC delay, 595 mW per channel digitisation
- 1 ns sampling time adjustment
- BCID (2 methods)
- Look-up table based calibration
- Histogramming, playback
- Jet-summing
- 400(480) Mbit/s serialisation
- 13 BC ticks from analog in to Jet (summed) serial output

Test 1. PHOS4 replacement: FPGA for time-adjustment



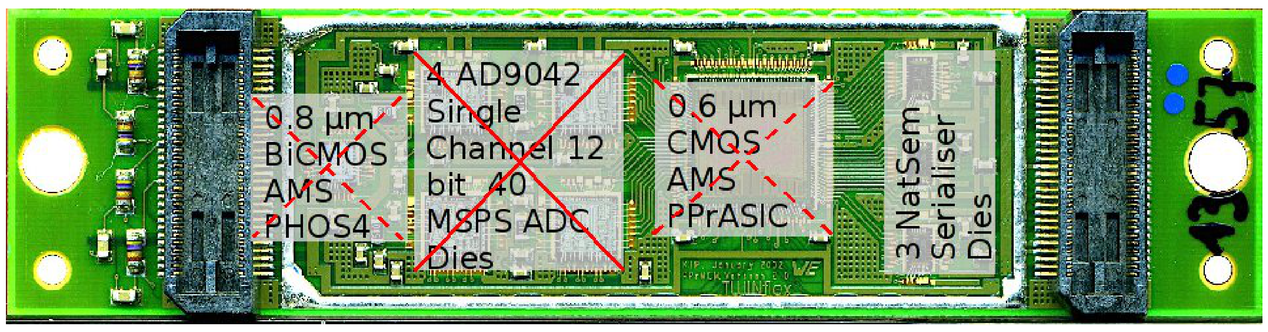


- AVNET development board with XC3S400A-4FTG256C Spartan-3A FPGA in the suitable for MCM package is used for testing
- PHOS4 chip task is fine time adjustment (resolution: 1 ns). This job can be done by FPGA's Digital Clock Manager (DCM):
  - Phase Shifter step is well bellow 1 ns
  - There are 8 DCMs in the XC3S1400A and 4 of them can be used for PHOS4 replacement (4 channels)

Conclusions

- New MCM (nMCM) can be built with the same form-factor and functionality
- Having a reconfigurable component (FPGA) we will gain in flexibility
- PHOS4 functionality and LVDS serialisers can be implemented inside FPGA $\Rightarrow$ less components on the module
- First tests shows that even Spartan-3A can be used
- Various FPGA evaluation boards, together with existing equipment for current MCM testing is used for development and tests before actual layout of the nMCM will be ready.

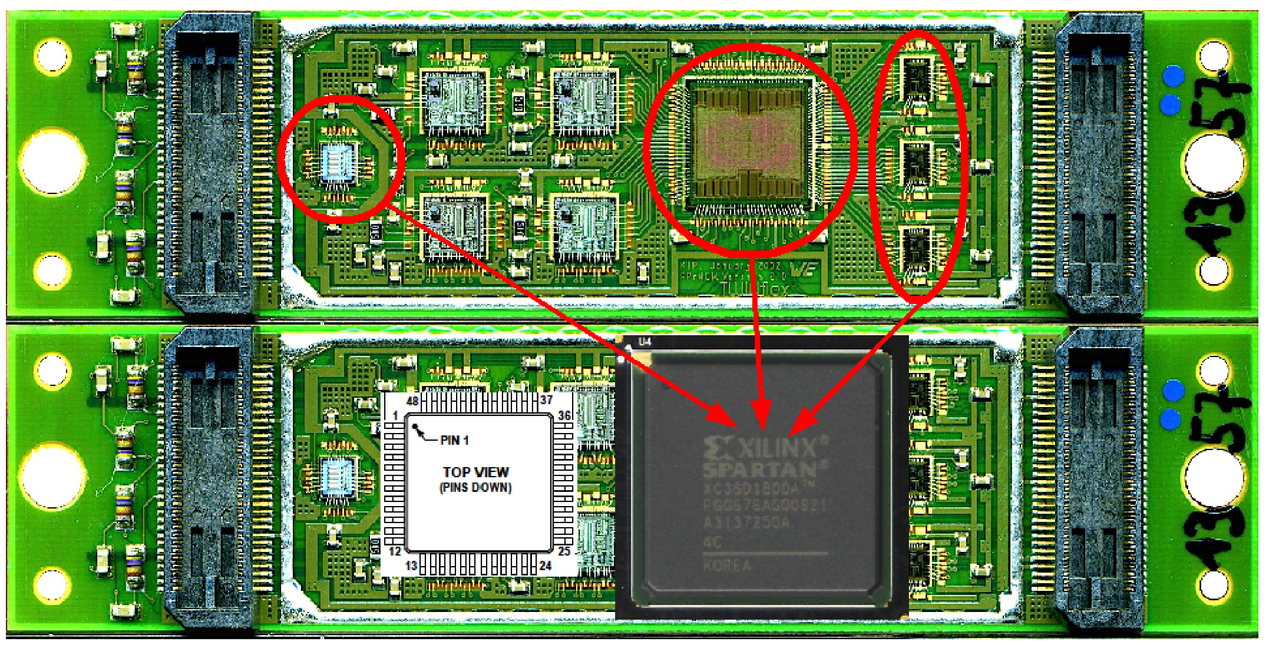
New MCM. Motivation.



VERY conservative spare policy(50%) has been implemented, but we would not be able to produce quickly more MCMs
9 ASIC Dies on each of 2048 MCMs in the System

- **PHOS4** (time-adjustment chip with 1ns resolution): GDSII available, process (still) available, success uncertain, no support
- **AD9042**: n/a as unpackaged die anymore, packaged version has prohibitive size
- **PPrASIC**: Verilog available, process (still) available, GDSII available, outdated technology ($0.6\mu m$)
- **Serialisers**: available, new pin compatible DS92LV1023E is recommended by NatSem

New MCM

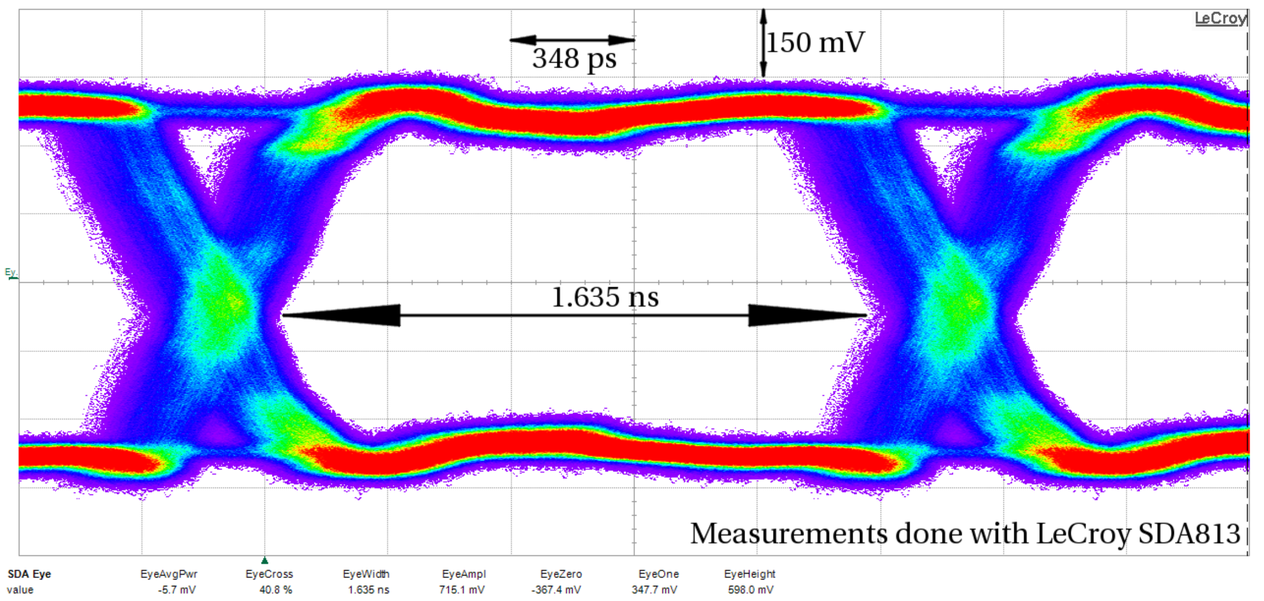


AD9218 Spartan AD9218

- We would like to develop a pin-, size- and latency-compatible substitute for the MCM based on todays components.
- Candidates for the main parts are two AD9218 (dual 105 MHz FADC) and a Spartan-3A(or Spartan-6)
  - Spartan-6 currently has limited availability
  - Spartan-3A (for ex. XC3S1400A) can be used for design and tests now
- Minimum components on board: 2 ADCs and FPGA – is it possible?

Test 2. LVDS serialisers in FPGA

480 Mbits/s: (10 data bits + 1 start bit + 1 stop bit) @ 40MHz
Eye-diagram shows a good signal quality confirming that even XC3S400A can be used as a serialiser:



Implemented using DDR I/O. 3 serialisers occupy <2% of the XC3S400A + 1 DCM