Chip Design and Test System Development in the VLDT Bonn

Overview and status of resources and current activities (Nov. 2009)

Chip Design Infrastructure

- ELA (in preparation)
- FE chip with reduced pixel size using modifications for TPC read
- Die size comparison FE extended local event storage
- IBM 130 nm clock management (PLL design)
- Wafer to wafer bonding by Tezzaron
- 3 chip design engineers + head of lab with support from VLDT Bonn

Environment

- ATLAS FE
- ADC
- High speed data transmission (LVDS drivers & receivers)
- DEPFET prototype DAQ system (HGF users: Heidelberg, power and bias generation (linear and shunt regulators, DACs)
- DCD
- Cadence, Synopsis and MentorGraphics software suites support higher data rates: new

Test beam technology pillar

- Test system for various prototype chips: GOSSIP 3, FE comprehensive test equipment, clean room etc.
- Status: prototype chip submitted in Summer 2009 (SPI interface, ADC read high speed data link test bench (20 GHz DSA + 3.35 GHz pattern generation)
- Common design effort: VLDT Bonn, CPPM, LBNL, supported technologies: IBM 130nm, IBM 90nm, UMC (div.)

DCD chip: multichannel digitizer, Switcher: line driver, DHP: digital two layer CMOS stack automatic and semi-automatic laser box (motor control)

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Chip Design Projects - Overview

Hybrid pixel detector front-end chip (ATLAS)
- Front-end chip upgrade for monolithic 4-layer (FE-I4)
- Reduced pixel size using 3D integration technology (FE-TICO)
- Clock control system (PLL)
- New power supply concepts (metal powering)

Gaseous Pixel Detectors

- Pixel chip development for tracking detectors and TPC read-out
- DEPFET Pixel Detector Belle II
- Test beam technology pillar
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Test stands and Prototype DAQ Systems

- Test stands for ASIC and sensor characterization
  - Automatic and semi-automatic wafer probe
  - Climate box
  - Laser box (three different wavelengths laser diodes)
  - Test beam chip test bench (2 GHz DDA + 3.35 GHz pattern generation)
- Test beam facilities (at ELA (in preparation))

DCD prototype DAQ system (top) and FE front-end system (bottom, bottom)

- DDD system development
  - DEPFET prototype DAQ system (HGF users: Heidelberg, Karlsruhe)
  - ATLS FE-I4 read-out system for single chip and water testing
  - DEPFET prototype DAQ system (HGF users: Heidelberg, Karlsruhe)
  - DEPFET prototype DAQ system (HGF users: Heidelberg, Karlsruhe)
  - Test system for various prototype chips: GOSSIP 3, FE-I4, TICO project