Chip Design and Test System Development in the VLDT Bonn

Overview and status of resources and current activities (Nov. 2009)

universitätbonn

Chip Design Infrastructure

Chip Design Resources in the VLDT Bonn

Personnel (chip design)
- 3 chip design engineers + head of lab
- 2-4 PhD and diploma students

Infrastructure
- chip designers office with 9 chip design workstations (7 permanent + **2 for guests users of the HGF Alliance**)
- supported technologies: IBM 130nm, IBM 90nm, UMC (div.), TSMC, AMS (div), Chartered/Tezzaron 130nm 3D etc.
- MPW access via Europractice and MOSIS
- Cadence, Synopsis and MentorGraphics software suites
- comprehensive test equipment, clean room etc.

Current Chip Design Projects - Overview

Hybrid pixel detector front-end chip (ATLAS)
- front-end chip upgrade for insertable B-Layer **(FE-I4)**
- FE chip with reduced pixel size using **3D integration** technology (FE-T/C4)
- detector control system **(DCS)**
- new power supply concepts **(serial powering)**

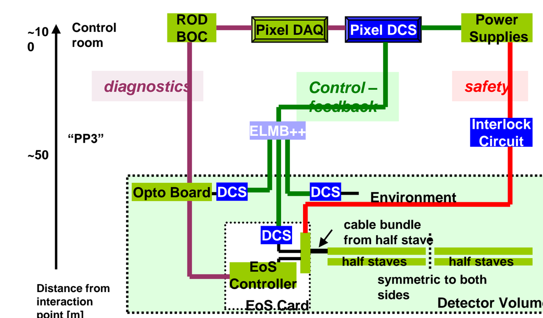
Gaseous pixel detector read-out (ILC)
- gas on slimmed silicon (GOSSIPO, tracking detector)
- modifications for TPC read-out @ ILC

DEPFET active pixel detector (BELLE 2)
- digital data handling processor **(DHP)**

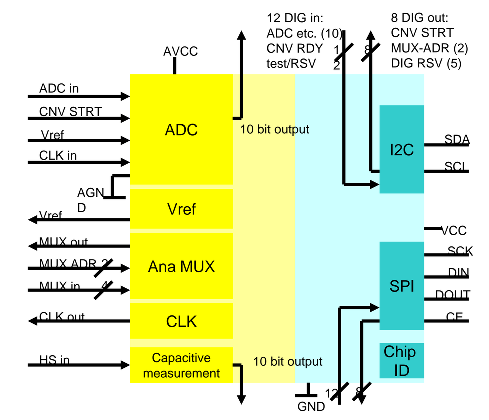
Compton Polarimeter (ELSA)
- counting micro-strip detector front-end chip

ATLAS Detector Control System

Upgrade for the ATLAS pixel detector (SLHC)
- development by **Uni Wuppertal** with support from VLDT Bonn
- integration of detector control functionality (DCS) on the end of stave
- status: prototype chip submitted in Summer 2009 (SPI interface, ADC, GPIO, hum. sensor)



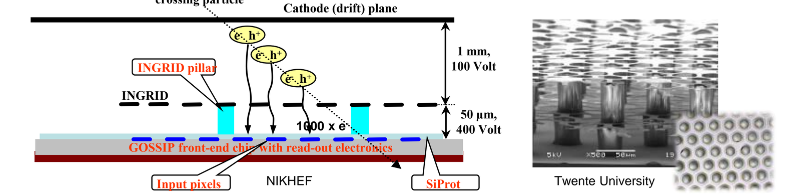
Proposed DCS layout for ATLAS upgrade



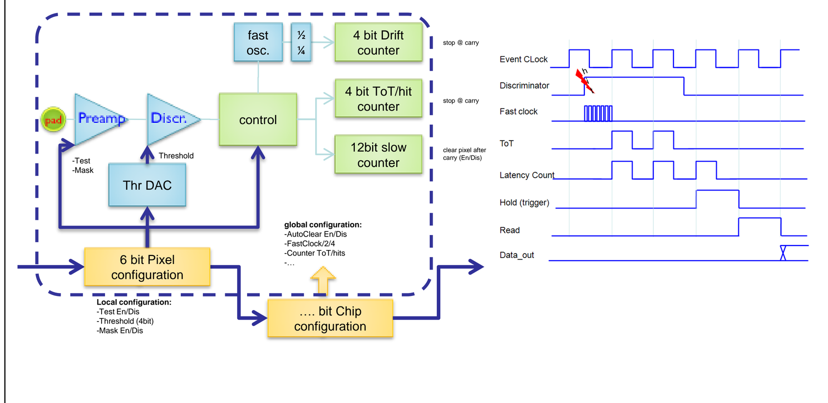
Block schematic of the DCS test chip

Gaseous Pixel Detectors

Pixel chip development for tracking detectors and TPC read-out
- GOSSIPO concept (NIKHEF): replace silicon sensor with thin gas layer for tracking applications
- with modifications also usable for **TPC read-out** (similar to TimePix)
- Bonn design tasks: optimized preamplifier, linear regulator for PLL control



GOSSIPO detector principle (left) and deposited gas amplification structure (INGRID, right)

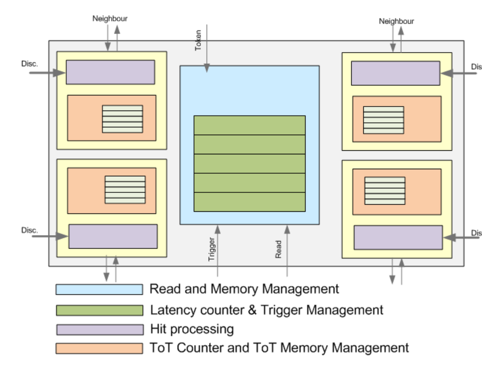


GOSSIPO pixel block diagram and signal timing

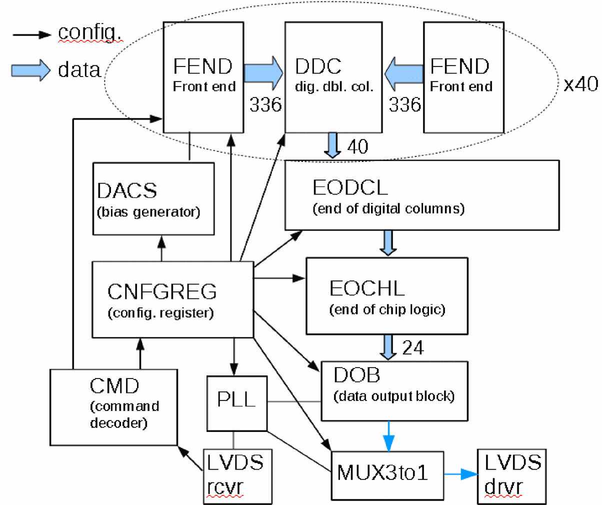
ATLAS Pixel Chip (FE-I4)

Upgrade for the ATLAS pixel detector
- target: insertable B-layer (**IBL**, phase 1 upgrade) and outer layers of **SLHC** (phase 2 upgrade)
- smaller pixel size: 400µm x 50 µm → **250 µm x 50 µm**
- **80 x 336 pixels**
- support higher data rates: new **digital column** architecture
- IBM 130 nm
- common design effort of VLDT Bonn, CPPM, Genua, LBNL, NIKHEF

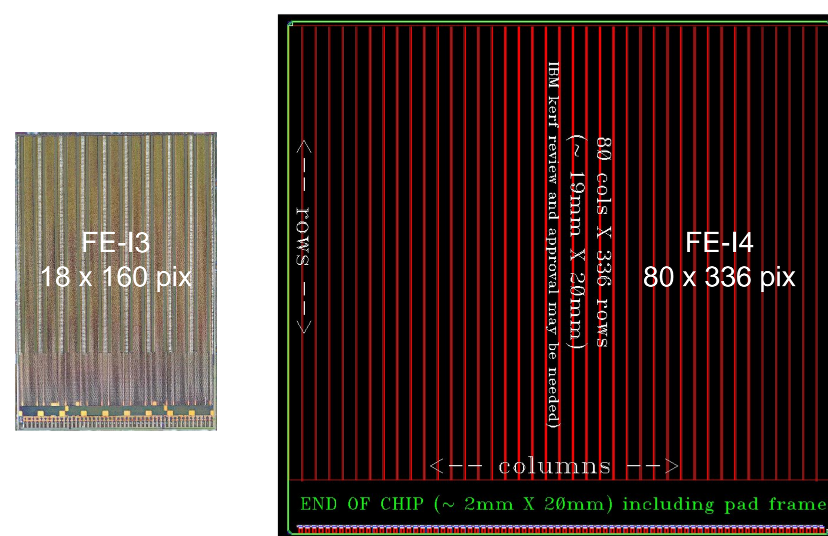
Bonn design tasks
- digital column
- high speed data transmission (LVDS drivers & receivers)
- clock management (PLL design)
- power and bias generation (linear and shunt regulators, DACs)



Block schematic and layout of a 2 x 2 pixel region (digital part)



Modular view of the FE-I4

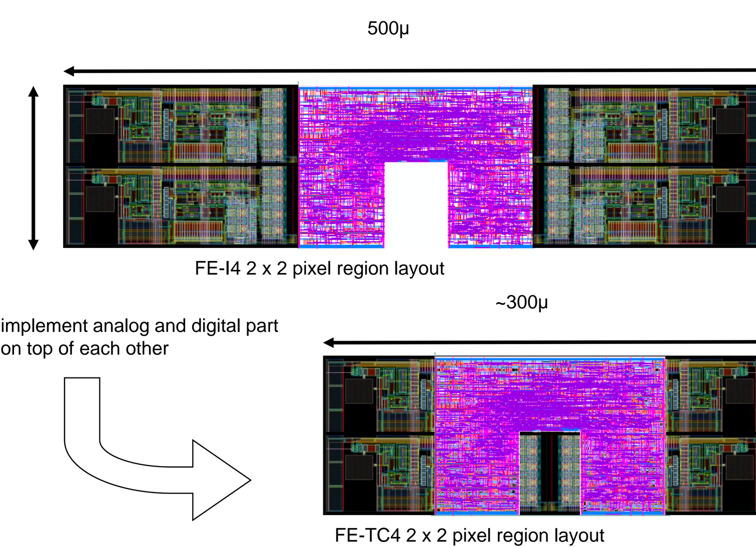


Die size comparison FE-I3 vs. FE-I4

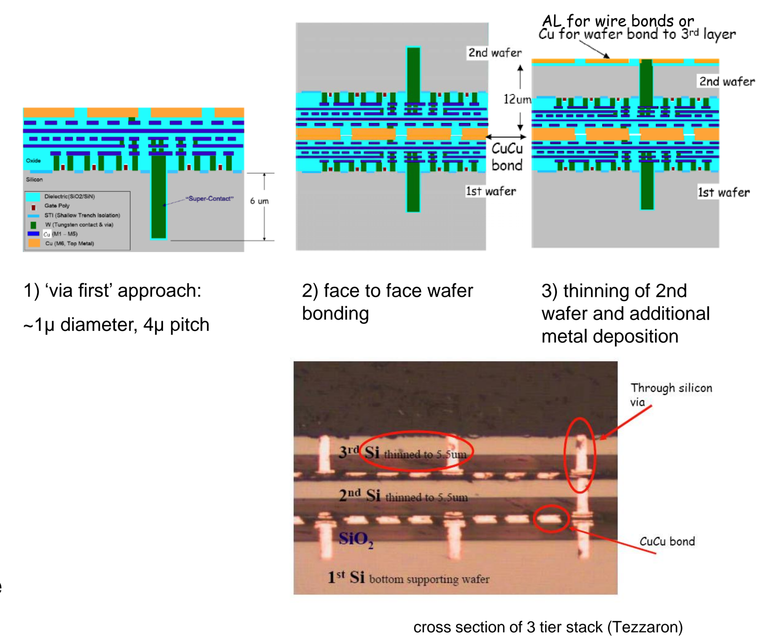
ATLAS Pixel Chip with Vertical Integration

Option for SHLC upgrade of the ATLAS pixel detector inner layer
- need for **smaller pixels** to reduce occupancy
- extended local event storage
- use **second CMOS layer** to separate analog and digital circuits on different layers → vertical **(3D) integration**
- common design effort: VLDT Bonn, CPPM, LBNL

Technology
- base process: Chartered 130 nm CMOS
- 'vias-first' approach
- two layer CMOS stack
- wafer to wafer bonding by Tezzaron
- MPW access via FNAL
- more than two tiers possible

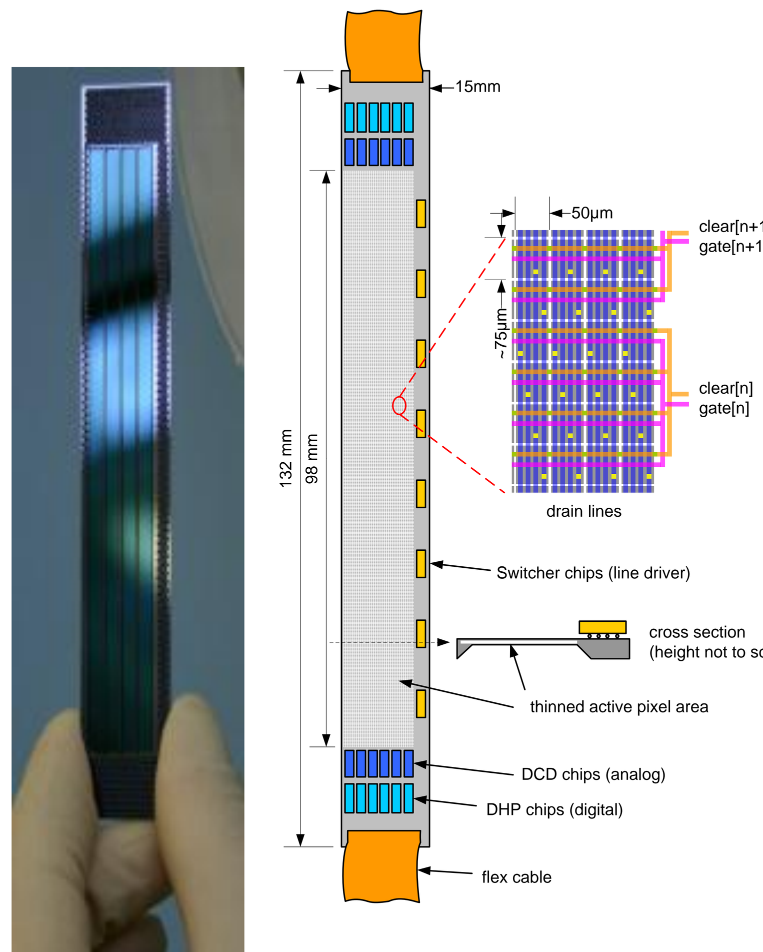


Conventional 2 x 2 pixel region layout of the FE-I4 (top) and possible size reduction for vertical integrated pixel region



Simplified processing steps for a two layer CMOS stack (top) and cross-section of a three layer stack

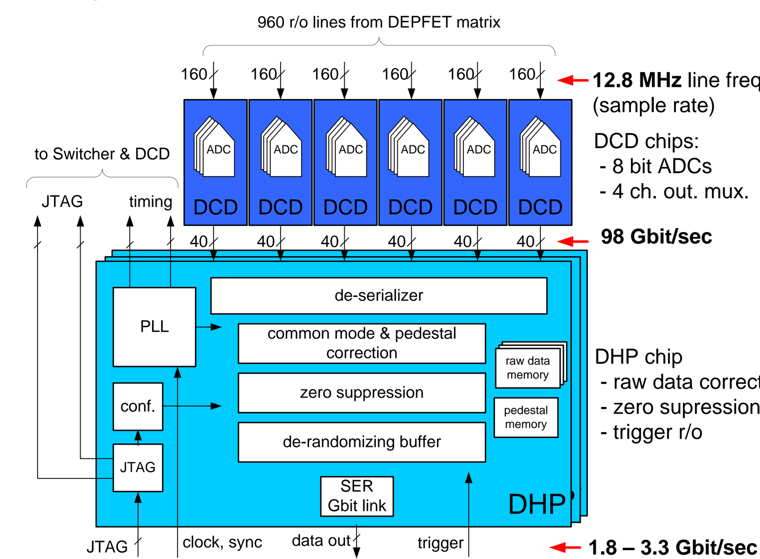
DEPFET Pixel Detector for Belle II



Picture (right) and conceptual drawing (left) of an 'all-silicon' DEPFET module for the BELLE 2 vertex detector (PXD)

DEPFET 'all silicon' pixel module
- read-out and control chips directly flip-chip mounted onto the sensor substrate
- DCD chip: multichannel digitizer, Switcher: line driver, DHP: digital data processor

Digital data handling processor (DHP)
- 90 nm technology
- data buffers, offset correction and zero-suppression
- clock management
- Multi-gigabit serializer and link
- design: VLDT Bonn and U Barcelona

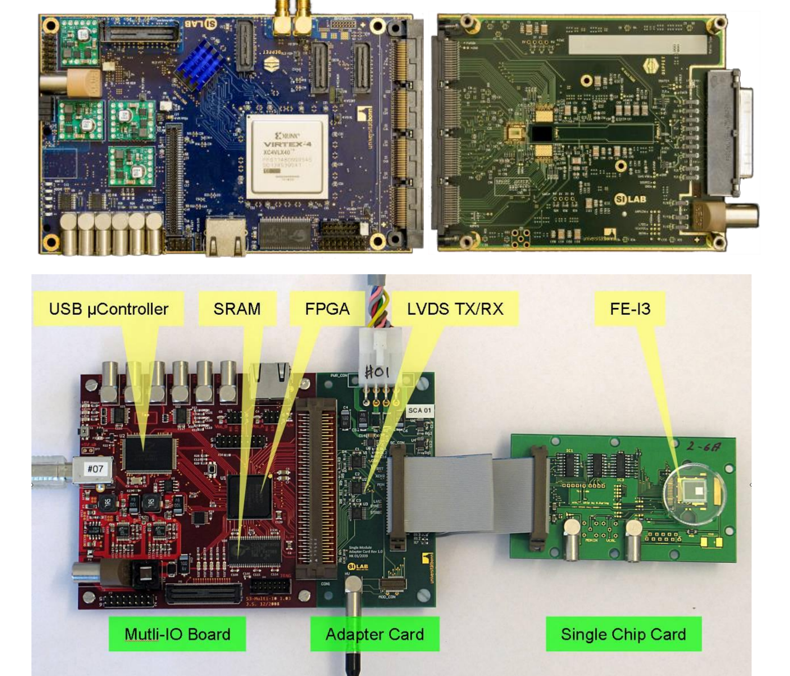


Functional block diagram of the data handling processor (DHP)

Test-stands and Prototype DAQ Systems

Test stands for ASIC and sensor characterization
- automatic and semi-automatic wafer prober
- climate box
- laser box (motor-table, three different wavelengths laser diodes)
- high speed data link test bench (20 GHz DSA + 3.35 GHz pattern generator)
- **Test beam** facility at ELSA (in preparation)

DAQ systems development
- DEPFET prototype DAQ system (HGF users: Heidelberg, Karlsruhe)
- ATLAS FE-I3/4 read-out system for single chip and wafer testing (HFG users: Dortmund, Göttingen, DESY, U Hamburg, HU Berlin)
- Compton polarimeter DAQ (ELSA)
- Test system for various prototype chips: GOSSIPO 3, FE-I4_proto1, FE-T/C4_proto1



DEPFET prototype DAQ system (top) and FE-I3/4 DAQ system (USBPix, bottom)

SI LAB Silizium Labor Bonn

LC-TPC

PHYSICS AT THE TERA SCALE Helmholtz Alliance

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