

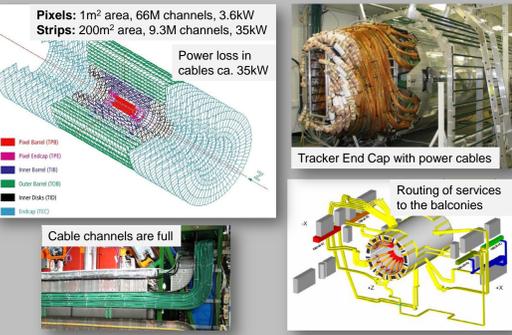
# Novel Powering Schemes for the CMS Tracker at the Super-LHC

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## The power distribution problem of the CMS tracker at the Super-LHC

### The CMS Tracker and its power distribution



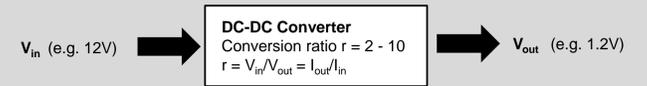
	LHC	SLHC Phase-1	SLHC Phase-2
Luminosity	$10^{34} \text{cm}^{-2}\text{s}^{-1}$	$2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$	$10^{35} \text{cm}^{-2}\text{s}^{-1}$
Particles in tracker	~ 1 000	~ 2 000	~ 15 000 – 20 000 depending on scenario
Start-up	2009 = $t_0$	$t_0 + 5$ years	$t_0 + 10$ years

### CMS Tracker power at the Super-LHC (SLHC)

- Higher granularity to keep occupancy at ~ 1%  $\Rightarrow$  shorter strips, more channels
- Track information must be used in the level-1 trigger to preserve trigger rate  $\Rightarrow$  pixelated layers with complex, fast digital electronics
- Smaller feature size front-end electronics: 250nm  $\rightarrow$  130nm or below  $\Rightarrow$  saves power, but leads to larger currents for same power consumption
- Improvement of detector performance by decreasing tracker material budget
- Services – including power cables – to the tracker cannot be accessed

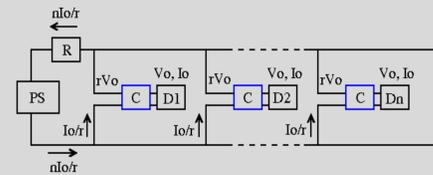
A new, different Tracker will be built. Its power consumption might be high.

## A possible solution: DC-DC conversion



### Parallel powering with DC-DC converters:

adopted by the CMS tracker as baseline in January 2009



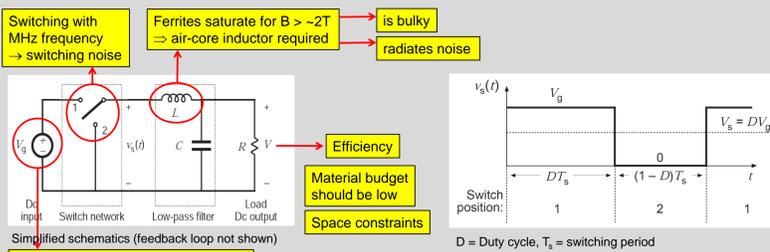
Resistive losses in cables  $P = R_{\text{cable}} \cdot I^2$  are reduced by a factor of  $1/r^2$ , e.g.  $r = 10 \Rightarrow$  losses reduced by  $1/100$

(Note: in praxis less reduction, since converter efficiency < 100%)

DC-DC converters are currently foreseen for the pixel detector at SLHC phase-1, and the outer tracker at SLHC phase-2.

## The DC-DC buck converter

- The simplest inductor-based step-down converter  $\Rightarrow$  few components  $\Rightarrow$  low mass
- Preferred because of its high efficiency (70-80%), the possibility to drive large output currents (several Amperes), and to provide high conversion ratios ( $r \sim 10$ )



Simplified schematics (feedback loop not shown)

Semi-conductor technology must stand  $V_{in} \approx 12V \rightarrow$  radiation-hardness

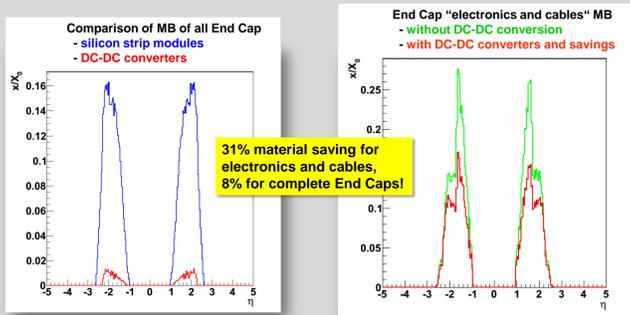
- Custom radiation-hard ASIC in non-standard technology is being developed by CERN-PH-ESE group
- Collaboration with CERN group since 2008, prototype chips already received and tested

## Aachen DC-DC buck converter development

- Development of converters with commercial, non radiation-hard buck converter ASICs
- Focus on low mass, low noise converter design, and study noise behaviour and integration aspects

## Tracker Material Budget with DC-DC conversion

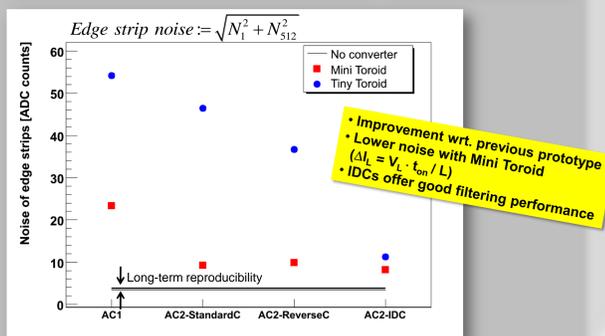
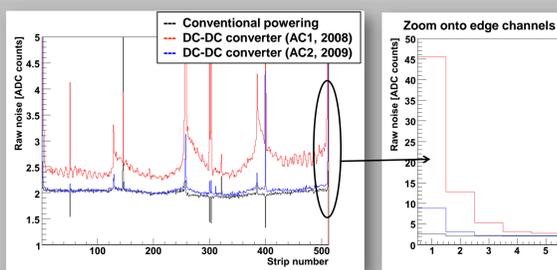
- Simulation of Tracker MB within CMS software (CMSSW), based on GEANT4
- One AC2-StandardC converter simulated per strip module, located on the front-end hybrid
- Assumptions: conversion ratio = 8, efficiency = 80%
- Copper savings in cables and motherboards evaluated based on tolerable voltage drop & power losses



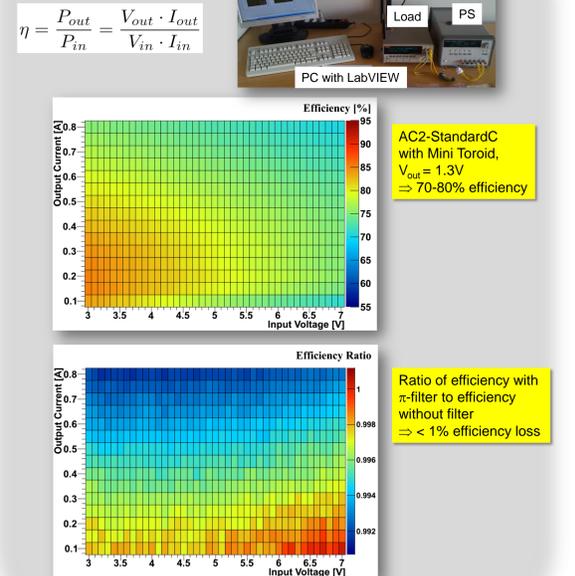
## Measurement of converter noise spectra

## System test measurements

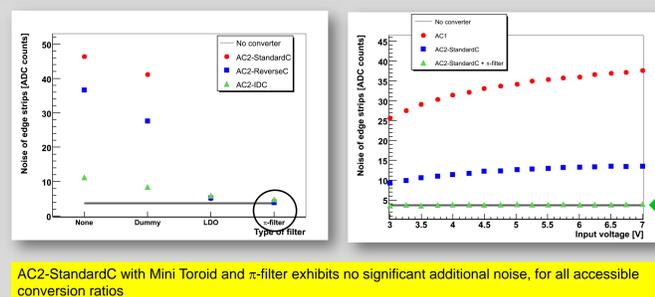
- New readout ASICs and modules prototypes not yet available
- A lot can already be learned from the operation of current tracker hardware with DC-DC converters



## Efficiency



## Filtering with additional filter boards



## Next steps

- Continue studies of noise coupling mechanisms
- Development of DC-DC converters using radiation-hard ASICs
- System tests with SLHC readout chips and prototype modules
- Converter integration aspects: cooling, space, shielding etc.

